

Serial No. 10/645,567

REMARKS

1. This paper is responsive to the office action of June 5, 2006.
- 5 2. In brief, the present invention is a method for verification of a processor model.
3. Claims 1-20 were pending in the application.
4. Claims 1 and 2 were rejected under 35 U.S.C. § 102(a) as being anticipated by
10 Huggins (US Pat. # 5,845,064). Claims 1 and 2 have been cancelled.
5. Claim 3 as objected to as being dependent upon a rejected base claim, but would
be allowable if rewritten in independent form including all of the limitations of the
base claim and any intervening claims. Claim 3 has been rewritten to include all
15 of the limitations of claims 1 and 2, and thus is now believed to now be in a
condition for allowance.
6. Claims 4-20 were allowed.
- 20 7. Claims 4 and 11 have been amended to correct typographical errors. No change
in scope of the claims has resulted, and no new matter has been added.
8. Since all rejected claims have been cancelled, and all objected to claims have been
rewritten, this application is considered to be in condition for allowance and such
25 action is earnestly solicited.

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Respectfully submitted,

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by 

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